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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/525,662	02/25/2005	Roelof Herman Willem Salters	NL 020797	9144

65913 7590 07/13/2007

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EXAMINER	
TRAN, ANTHAN	

ART UNIT	PAPER NUMBER
2827	

NOTIFICATION DATE	DELIVERY MODE
07/13/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/525,662	SALTERS ROEL	
	Examiner	Art Unit	
	Anthan T. Tran	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 07/02/2007 has been entered.

Response to Amendment

2. Applicant's response filed on July 02, 2007 in which claims 1 was amended have been entered of record.

Specification

3. The disclosure is objected to because of the following informalities: The specification fails to have headings for BACKGROUND OF THE INVENTION, SUMMARY OF THE INVENTION, and BRIEF DESCRIPTION OF THE DRAWINGS.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida et al. (US Pub. 2003/0021168) in view of Tomita et al. (US Pub. 2003/0156485) and further in view of Haddad et al. (US Pat. 6,275,415).

Regarding claim 1, Fig. 1 of Ishida discloses a static semiconductor device comprising: a matrix of static memory cells [3] functionally arranged in rows and columns, bit line circuits [BL1-BLn#, 6, 12, 14], each for writing memory cells in a respective one of the column, a word line circuit [WL1, 4] constructed so that the word line is capable of selecting memory cells in a plurality of the rows to receive write data from the bit line driver circuits, and a cell strength control circuitry [11] coupled to the cells [3] and arranged to reduced write strengths required to write data into individual ones of the memory cells [paragraphs 0057, 0058], relative to a drive strength of the bit line circuits [paragraph 0058].

Ishida fails to discloses selecting plurality of rows simultaneously. However, paragraph 0080 of Tomita discloses a static random access memory that selecting plurality of rows simultaneously, and reduce power consumption even if number of rows are selected.

Ishida in view of Tomita discloses all claimed invention, but does not specifically disclose reduced drive strength in dependence of number of cells simultaneously

programming. However, Haddad discloses reducing drive strength when more cells are programming simultaneously (in dependence of number of cells programming) [col. 5, lines 31-41].

Since Ishida, Tomita and Haddad are both from the same field of memory device, the purpose discloses by Tomita and Haddad would have been recognized in the pertinent art of Ishida.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to make a memory device capable of selecting plurality of rows simultaneously, and reduced drive strength in accordance to number of cells program silmultaneously. The ordinary artisan would have been motivated to modify Ishida in the manner set forth above in order to supply the right voltage to memory cells to have stable high-speed operation

Regarding claims 2 and 7, Fig. 1 of Ishida discloses wherein the cell strength control circuitry [11] comprises a plurality of power supply reduction circuits [as shown in Fig. 2 and 5], each coupled between a common power supply [Vcc, Fig. 2] and a respective internal power supply line [out, Fig. 2], the memory cells [3] in respective ones of the columns each having power supply inputs [Vccin] coupled a respective one of the internal power supply lines [out], each power supply reduction circuit being arranged to provide a respective power supply voltage drop on the respective one of the internal power supply lines to which that power supply reduction circuit is coupled [0058], selectively at least during writing of data into the memory cells [0073, during writing and reading operation].

Regarding claims 3-4 and 8, Fig. 2 of Ishida discloses wherein the power supply reduction circuit [11A] comprises a resistive element [transistor T1] coupled between the common power supply [Vcc] and the internal power supply line [out].

Regarding claims 5 and 9, Fig. 1 of Ishida discloses wherein the bit line circuit for the at least one of the columns comprises a bit-line driver circuit [12, 12 is an precharging circuit that drives voltage to the bit line (BL1-BLn#)] with a power supply input [Vcc] coupled to the internal power supply line [Vccin].

Regarding claims 6 and 10, Fig. 6 of Ishida discloses wherein the bit-line driver circuit has a control input [122B, paragraph 0079] to receive a control voltage [Vcc – threshold voltage of 121B] from the common power supply line [Vcc], substantially unaffected by said drop.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthan T. Tran whose telephone number is 571-272-8709. The examiner can normally be reached on M-F, 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, AMIR ZARABIAN can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Anthan Tran
AT

HUAN HOANG
PRIMARY EXAMINER